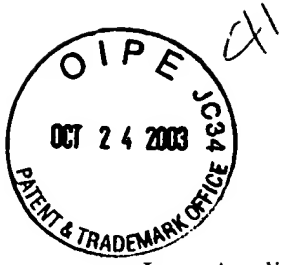


2829



Docket No.: 50090-265
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277
Kiyotoshi UEDA, et al. : Confirmation Number: 1553
Serial No.: 09/766,845 : Group Art Unit: 2829
Filed: January 23, 2001 : Examiner: P. Patel

**For: METHOD AND APPARATUS FOR TESTING SEMICONDUCTOR
INTEGRATED CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT
MANUFACTURED THEREBY**

RESPONSE TO RESTRICTION REQUIREMENT

Mail Stop Restriction Requirement
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RECEIVED
OCT 28 2003
TC 2800 MAIL ROOM

Noting the Office Action dated September 24, 2003 wherein restriction has been required, Applicants hereby provisionally elect Group I (claims 1-5 and 13, drawn to semiconductor integrated testing method) for prosecution in the above-identified application, with traverse.

REMARKS

MPEP §811 states that the Examiner “should make a proper requirement as early as possible in the prosecution, in the first action if possible, otherwise, as soon as the need for a proper requirement develops.” In the first action, the Examiner made a requirement to restrict between species, to which Applicants elected without traverse. After examining the claims on